ABSTRACT OF THE DISCLOSURE

In a clock recovery circuit, the output clock from a voltage controlled oscillator is delayed and then provided to a phase detector circuit that generates a difference signal indicating the phase difference between an incoming data stream and the delayed output clock. A loop filter circuit receives the difference signal and supplies a control signal to the oscillator circuit, which varies the output clock according to the control signal. A delay clock circuit receives a delay control signal derived from the difference signal to determine the output clock delay.